APPENDIX A

1 (Currently Amended). A method for providing simultaneous bidirectional signaling in a bus topology comprising the steps of:

selecting a first memory device and a second memory device from among a plurality of memory devices ~~operably~~ coupled to a common bus line to exchange a first set of data;

scheduling a first exchange slot over which the first memory device and the second memory device are to exchange the first set of data; and

during the first exchange slot, simultaneously transmitting a first portion of the first set of data from the first memory device to the second memory device over the common bus line and transmitting a second portion of the first set of the data from the second device to the first device over the common bus line.

2 (Currently Amended). The method of claim 1 further comprising the steps of:

selecting the first memory device and a third memory device to exchange a second set of data;

scheduling a second exchange slot over which the first memory device and the third memory device are to exchange the second set of data; and

during the second exchange slot, simultaneously transmitting a first portion of the second set of data from the first memory device to the third memory device over the common bus line and transmitting a second portion of the second set of the data from the third memory device to the first memory device over the common bus line.

3 (Original). The method of claim 2 further comprising the step of:

introducing a turnaround delay between the first exchange slot and the second exchange slot.

4 (Currently Amended). The method of claim 3 wherein the turnaround delay is less than twice an end-to-end propagation delay of the common bus line.

5 (Currently Amended). The method of claim 1 wherein the first memory device is a memory controller device, and the second memory device is a memory storage device and wherein the first portion of the first set of data and the first portion of the second set of data are write data and the second portion of the first set of data and the second portion of the second set of data are read data.

6 (Currently Amended). A system for providing simultaneous bidirectional signaling ~~using~~ in a bus topology, the system comprising:

a first memory device ~~operably~~ coupled to a bus line;

a second memory device ~~operably~~ coupled to the bus line, the first memory device transmitting a first portion of a first set of data over the bus line to the second memory device and the second memory device transmitting a second portion of the first set of data over the bus line to the first memory device simultaneously during a first exchange slot; and

a third memory device ~~operably~~ coupled to the bus line, the first memory device transmitting a first portion of a second set of data over the bus line to the third memory device and the third memory device transmitting a second portion of the second set of data over the bus line to the first memory device simultaneously during a second exchange slot.

7 (Original). The system of claim 6 wherein a turnaround delay exists between the first exchange slot and the second exchange slot.

8 (Currently Amended). The system of claim 7 wherein the

turnaround delay is less than twice an end-to-end propagation delay ~~of~~ associated with the bus line.

9 (Currently Amended). The system of claim 6 wherein the first memory device is a memory controller device, and the second memory device is a memory storage device and wherein the first portion of the first set of data and the first portion of the second set of data are write data and the second portion of the first set of data and the second portion of the second set of data are read data.

10 (Currently Amended). A memory device coupled to a bus line in a bus topology for providing simultaneous bidirectional signaling, the memory device comprising:

a ~~driver~~ transmitter circuit configured to provide additive signaling, the ~~driver~~ transmitter circuit applying transmit signals to the bus line;

a receiver circuit operably coupled to the ~~driver~~ transmitter circuit, the receiver circuit configured to effectively subtract the transmit signals to receive received signals from the bus line, the ~~driver~~ transmitter circuit and the receiver circuit operating during an exchange slot.

11 (Currently Amended). The memory device of claim 10 wherein the memory device is coupled to the bus line by an impedance-matching splitter.

12 (Currently Amended). The memory device of claim 10 wherein the memory device further comprises:

a terminator operably coupled to the ~~driver~~ transmitter circuit and the receiver circuit, the terminator providing a controlled termination impedance.

13 (Currently Amended). The memory device of claim 10 wherein the ~~device~~ transmitter circuit further comprises:

a driver operably coupled to the bus line, the driver configured to apply the transmit signals to the bus line using additive signaling; and

a transmitter ~~circuit~~ operably coupled to the driver, the transmitter providing the transmit signals to the driver ~~circuit comprising a transmit buffer, the transmit buffer holding data pending arrival of the exchange slot~~.

14 (Currently Amended). The memory device of claim 13 wherein the ~~transmit buffer~~ transmitter circuit further comprises:

a plurality of transmit buffers operably coupled to the

transmitter, the plurality of transmit buffers configured to hold data destined for different other memory devices.

15 (Currently Amended). The memory device of claim 13 wherein the receiver circuit further comprises:

a comparator operably coupled to the transmitter, ~~and to~~ the driver, and the bus line, the comparator configured to effectively subtract the transmit signals to yield received signals from the bus line; and

a receiver operably coupled to the comparator, the receiver receiving the received signals and obtaining received data from the received signals.

16 (Currently Amended). The memory device of claim 15 further comprising:

an enabling circuit, coupled to the transmit circuit and the receive circuit, responsive to an exchange slot indication, the enabling circuit enabling the operation of the transmit circuit and the receive circuit during the exchange slot.

17 (Currently Amended). A memory system comprising:

a memory controller;

a bus line ~~operably~~ coupled to the memory controller;

a first memory device ~~operably~~ coupled to the bus line, the first memory device configured to simultaneously send first read data to the memory controller via the bus line and receive first write data from the memory controller via the bus line; and

a second memory device ~~operably~~ coupled to the bus line, the second memory device configured to simultaneously send second read data to the memory controller via the bus line and receive second write data from the memory controller via the bus line.

18 (Previously Presented). The memory system of claim 17 wherein the first memory device is configured to simultaneously send the first read data to the memory controller and receive the first write data from the memory controller during a first exchange slot and wherein the second memory device is configured to simultaneously send the second read data to the memory controller and receive the second write data from the memory controller during a second exchange slot.

19 (Original). The memory system of claim 18 wherein the memory controller comprises:

a first write buffer to hold the first write data pending arrival of the first exchange slot.

20 (Original). The memory system of claim 19 wherein the memory controller comprises:

a second write buffer to hold the second write data pending arrival of the second exchange slot.

21 (Currently Amended). The memory system of claim 17 wherein the bus line comprises:

a conductor ~~operably~~ coupling the first memory device and the second memory device to the memory controller, wherein the first memory device is configured to simultaneously send a first read bit of the first read data to the memory controller over the conductor and receive a first write bit of the first write data from the memory controller over the conductor during a first exchange slot and wherein the second memory device is configured to simultaneously send a second read bit of the second read data to the memory controller over the conductor and receive a second write bit of the second write data from the memory controller over the conductor during a second exchange slot.

22 (Original). The memory system of claim 21 wherein a turnaround delay sufficient to prevent inter-symbol interference

is introduced between the first exchange slot and the second exchange slot.

23 (Original). The memory system of claim 17 wherein the memory controller performs coherency checking during memory access operations.

24 (Currently Amended). A memory device comprising:

a ~~driver~~ transmitter circuit configured to drive a bus line with read data during an exchange slot while write data ~~are~~ is present on the bus line;

a receiver circuit operably coupled to the ~~driver~~ transmitter circuit, the receiver circuit configured to receive the write data from the bus line during the exchange slot while the ~~driver~~ transmitter circuit is driving the bus line with the read data; and

a memory circuit operably coupled to the transmitter circuit and the receiver circuit, the memory circuit configured to provide the read data and to store the write data.

25 (Currently Amended). The memory device of claim 24 further comprising:

an enabling circuit responsive to an exchange slot

indication, the enabling circuit operably coupled to the ~~driver~~ transmitter circuit and the receiver circuit, the enabling circuit enabling interaction of the ~~driver~~ transmitter circuit and the receiver circuit with the bus line during the exchange slot.

26 (Previously Presented). The memory device of claim 25 wherein the enabling circuit is configured to be responsive to the exchange slot indication following a turnaround delay sufficient to prevent inter-symbol interference.

27 (Currently Amended). The memory device of claim 24 ~~further comprising:~~

~~a transmit circuit operably coupled to the driver,~~ wherein the transmitter circuit ~~comprising~~ further comprises:

a driver operably coupled to the bus line, the driver configured to drive the bus lines with the read data using additive signaling;

a transmitter operably coupled to the driver, the transmitter providing the read data to the driver; and

a transmit buffer operably coupled to the transmitter, the transmit buffer holding the read data pending arrival of the exchange slot.

28 (Currently Amended). A memory controller comprising:

a ~~driver~~ transmitter circuit configured to drive a bus line with first write data destined for a first memory device during a first exchange slot while first read data from the first memory device ~~are~~ is present on the bus line; and

a receiver circuit operably coupled to the ~~driver~~ transmitter circuit, the receiver circuit configured to receive the first read data from the bus line during the first exchange slot while the ~~driver~~ transmitter circuit is driving the bus line with the first write data.

29 (Currently Amended). The memory controller of claim 28 wherein the ~~driver~~ transmitter circuit is further configured to drive the bus line with second write data destined for a second memory device during a second exchange slot while second read data from the second memory device ~~are~~ is present on the bus line and wherein the receiver circuit is further configured to receive the second read data from the bus line during the second exchange slot while the ~~driver~~ transmitter circuit is driving the bus line with the second write data.

30 (Original). The memory controller of claim 29 wherein a

turnaround delay sufficient to prevent inter-symbol interference is introduced between the first exchange slot and the second exchange slot.

31 (Currently Amended). The memory controller of claim 28 wherein the transmitter circuit further ~~comprising~~ comprises:

a driver operably coupled to the bus line, the driver configured to drive the bus line with the first write data using additive signaling; and

a transmitter ~~circuit~~ operably coupled to the driver to transmit the first write data ~~and the second write data~~ to the driver~~, the transmit circuit comprising a transmit buffer to hold the first write data pending arrival of the first exchange slot and the second write data pending arrival of the second exchange slot~~.

32 (Currently Amended). The memory controller of claim 31 wherein the ~~transmit buffer~~ transmitter circuit further comprises:

a first transmit buffer to hold the first write data pending arrival of the first exchange slot; and

a second ~~memory~~ transmit buffer to hold the second write data pending arrival of the second exchange slot.

33 (Currently Amended). A method for providing simultaneous bidirectional communication between a memory controller and a plurality of memory devices comprising the steps of:

during a first exchange slot, simultaneously communicating over a common bus line first write data from the memory controller to a first memory device of the plurality of memory devices and first read data from the first memory device to the memory controller; and

during a second exchange slot, simultaneously communicating over ~~a~~ the common bus line second write data from the memory controller to a second memory device of the plurality of memory devices and second read data from the second memory device to the memory controller.

34 (Original). The method of claim 33 further comprising the step of:

holding the first write data destined for the first memory device in the memory controller pending arrival of the first exchange slot.

35 (Original). The method of claim 34 further comprising the step of:

holding the second write data destined for the second memory device in the memory controller pending arrival of the second exchange slot.

36 (Original). The method of claim 35 wherein the step of holding the first write data occurs in a first write buffer and wherein the step of holding the second write data occurs in a second write buffer.

37 (Original). The method of claim 35 further comprising the steps of:

holding the first read data destined for the memory controller in the first memory device; and

holding the second read data destined for the memory controller in the second memory device.

38 (Currently Amended). The method of claim 37 wherein the step of simultaneously communicating over the common bus line the first write data from the memory controller to the first memory device and the first read data from the first memory device to the memory controller occurs after a specified amount of the first write data destined for the first memory device is held in the memory controller.

39 (Currently Amended). A system for bidirectional communication of data over a common bus line comprising:

a first device operably coupled to the common bus line, the first device comprising a first-to-second transmit buffer to hold first-to-second data and a first-to-third transmit buffer to hold first-to-third data;

a second device operably coupled to the common bus line, the second device comprising a second-to-first transmit buffer to hold second-to-first data;

a third device operably coupled to the common bus line, the third device comprising a third-to-first transmit buffer to hold third-to-first data; and

a scheduler operably coupled to the common bus line, the scheduler scheduling the first device to transmit the first-to-second data and the second device to transmit the second-to-first data over the common bus line simultaneously during a first exchange slot and scheduling the first device to transmit the first-to-third data and the third device to transmit the third-to-first data over the common bus line simultaneously during a second exchange slot, the scheduler introducing a turnaround delay sufficient to prevent inter-symbol

interferences between the first exchange slot and the second exchange slot.